CSCI 210: Computer Architecture
Lecture 20: Clocks, Latches and Flip-Flops

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Slides from Cynthia Taylor

Announcements

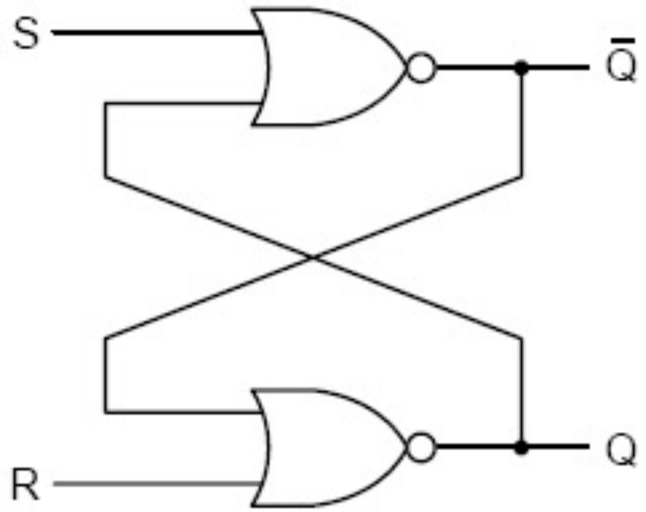
- Problem Set 6 due Friday

- Lab 5 due a week from Sunday

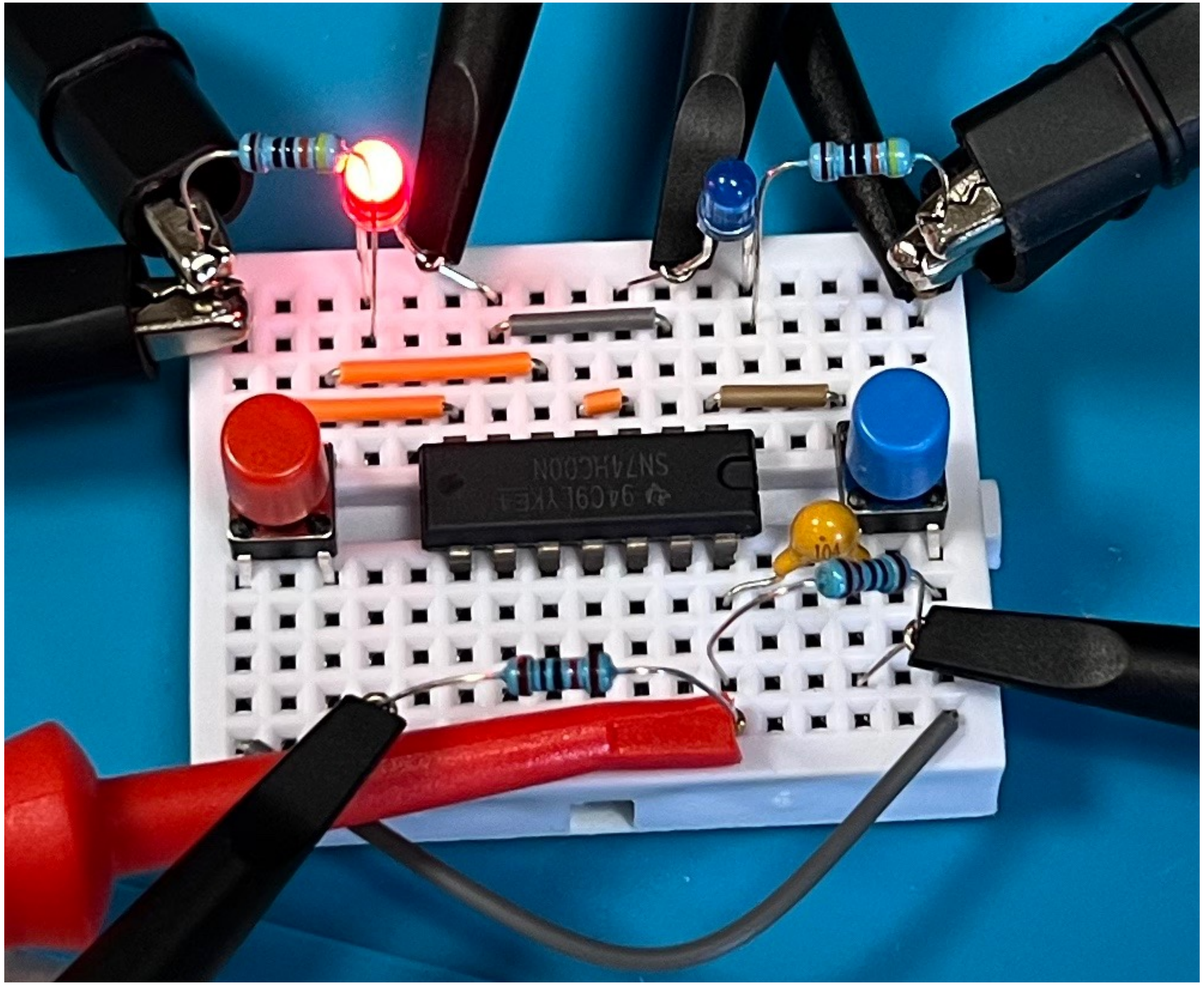
- Office Hours Friday 13:30–14:30

S-R Latch

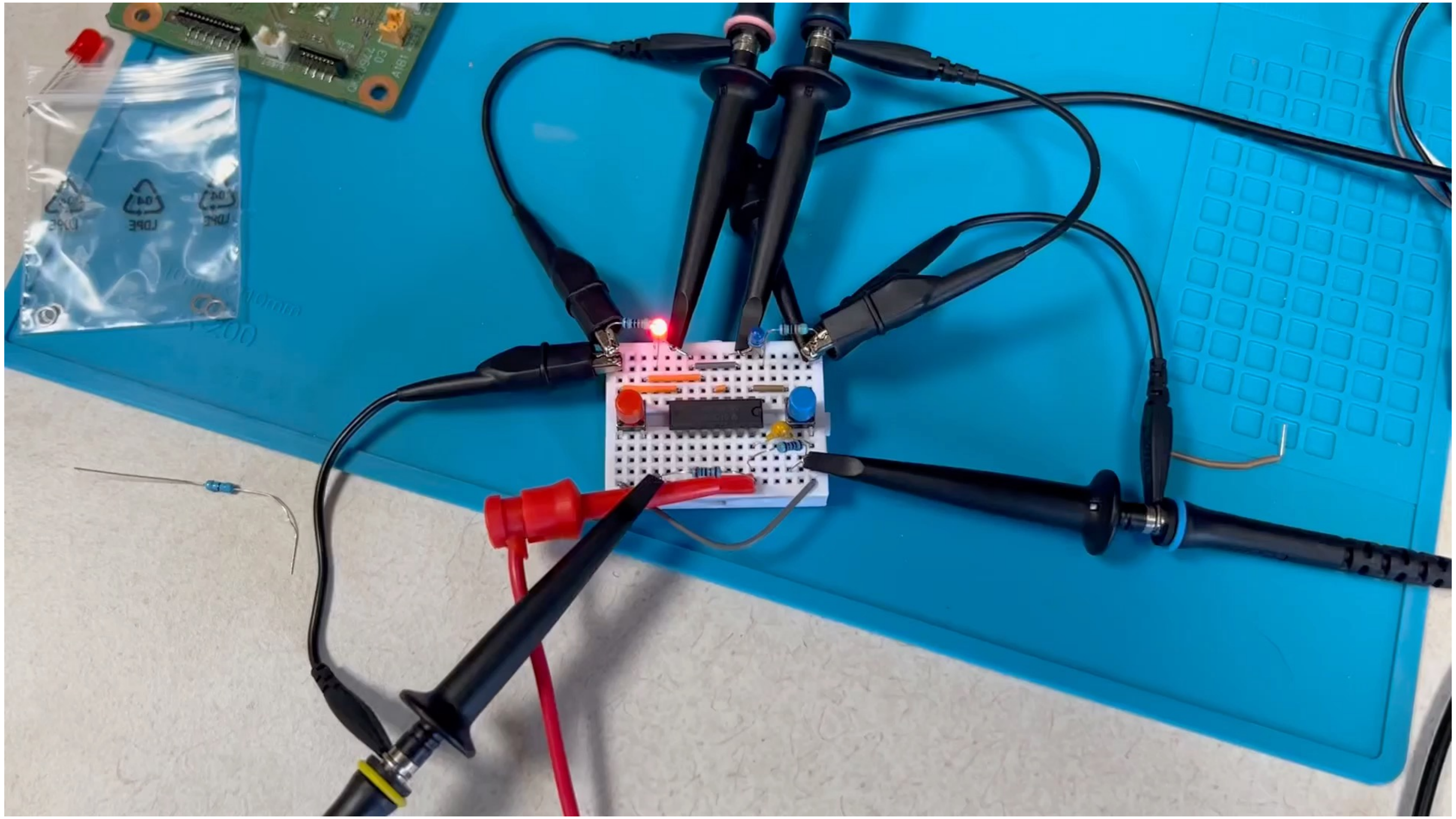
- Set: $Q_t = 1$ $\bar{Q}_t = 0$
- Reset: $Q_t = 0$ $\bar{Q}_t = 1$
- Otherwise: $Q_t = Q_{t-1}$ $\bar{Q}_t = \bar{Q}_{t-1}$



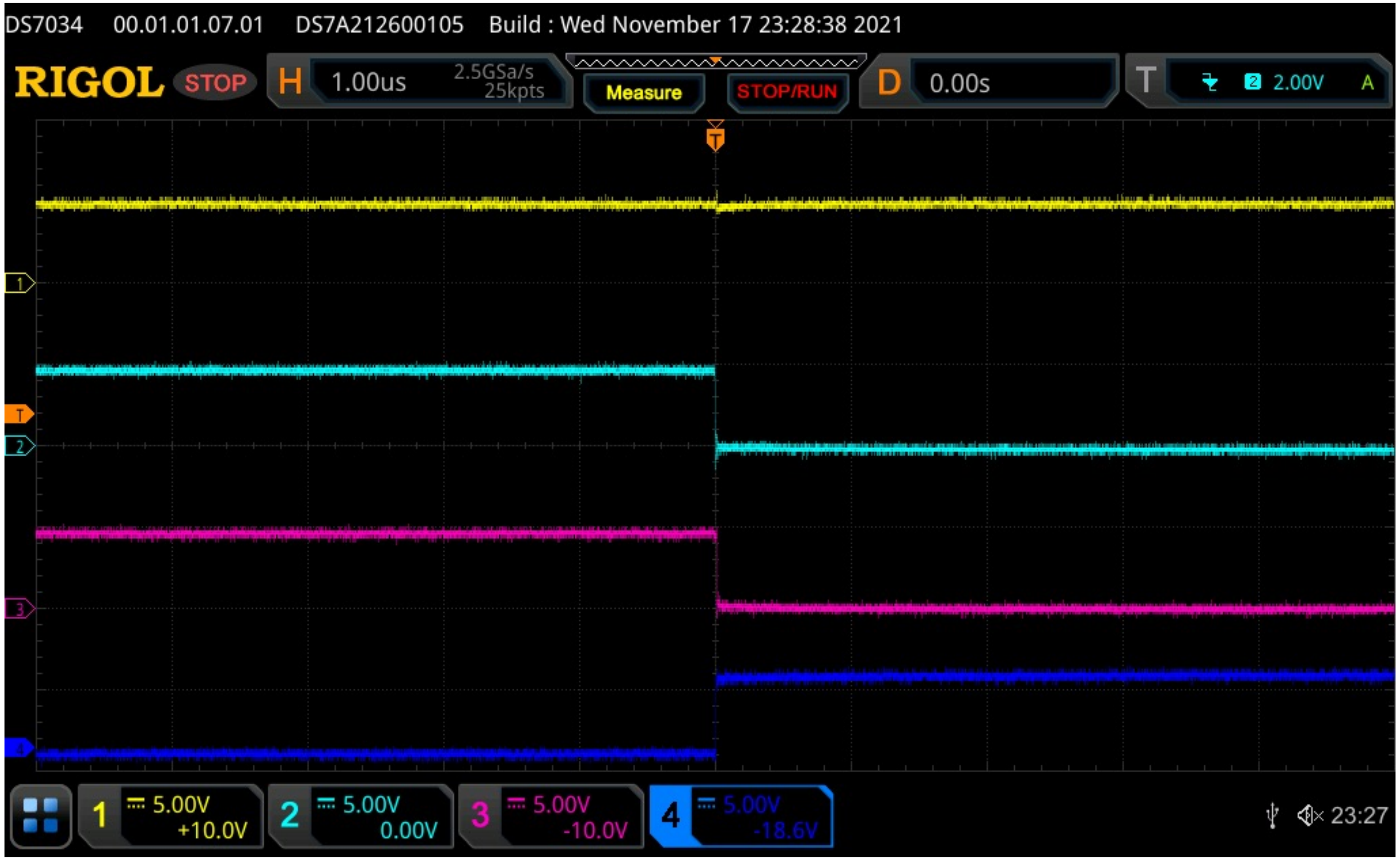
We can also build S-R latches out of NAND gates



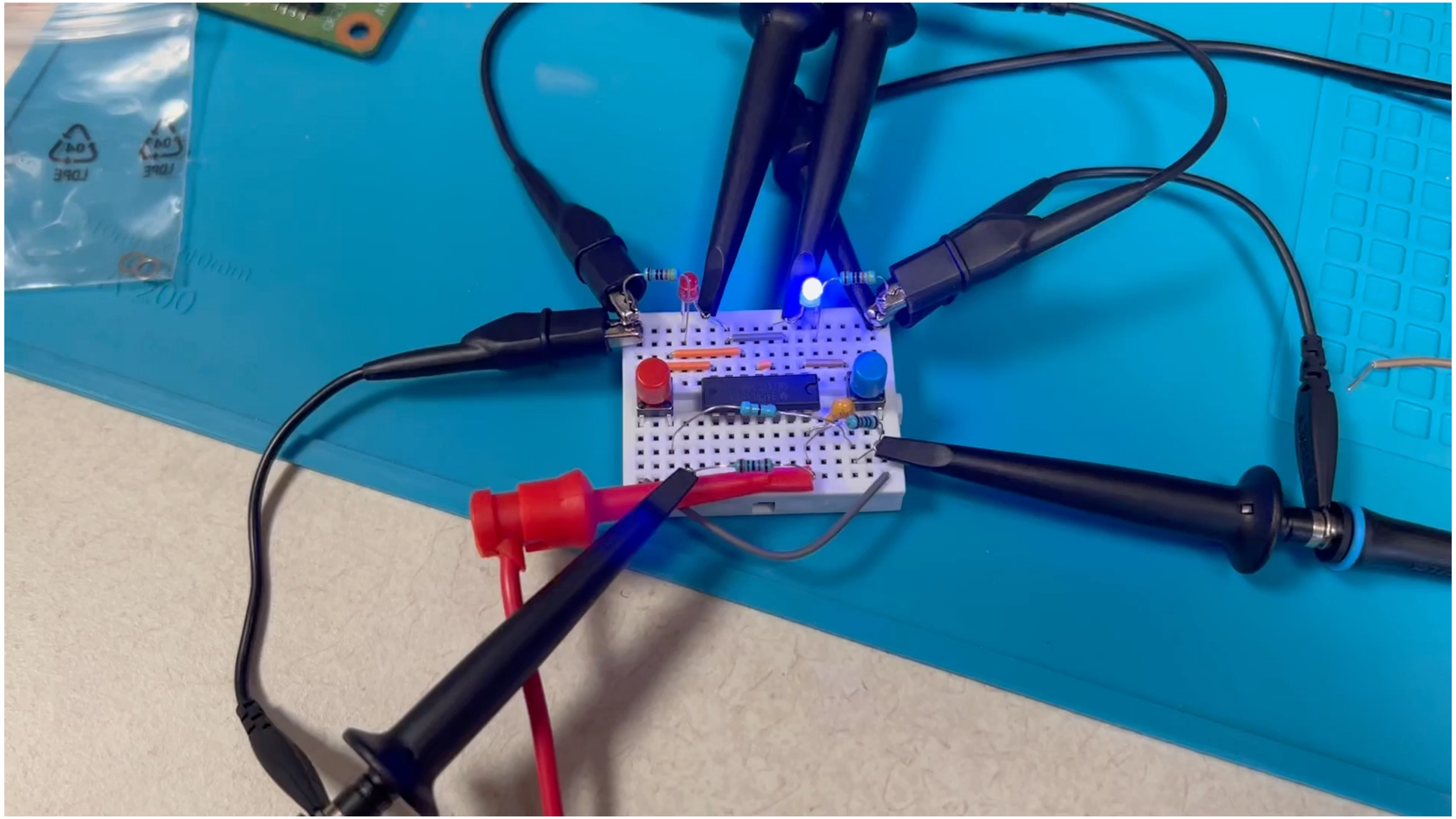
The logic is inverted: set and reset are 0-triggered



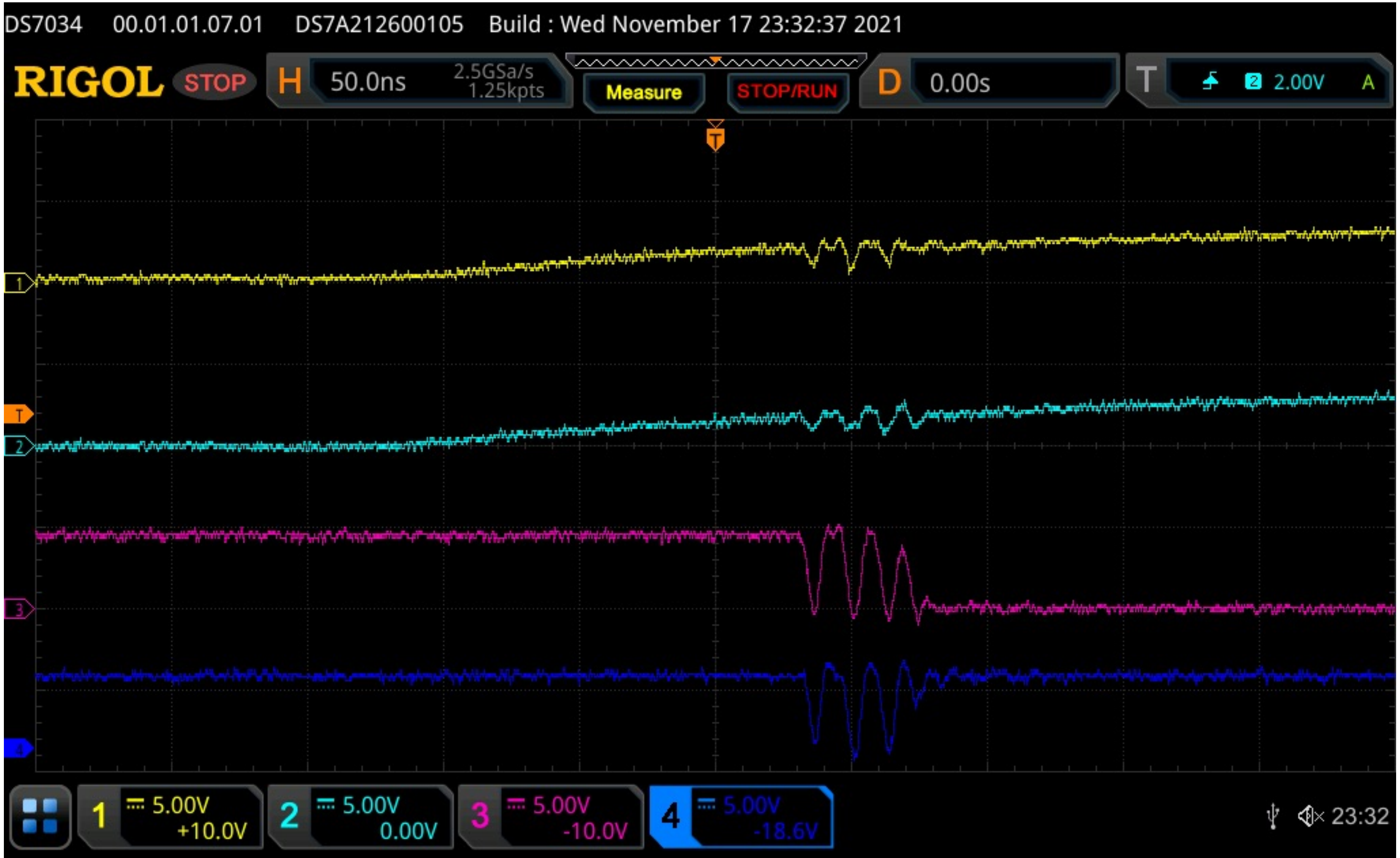
The logic is inverted: set and reset are 0-triggered



S = 0, R = 0 is the invalid combination



When S and R are released (brought to 1) simultaneously, it’s astable



Clock

- Oscillates between 1 and 0 with a fixed period
  - 0 to 1 transition is a **rising edge**
  - 1 to 0 transition is a **falling edge**
  - Time between two rising (or falling) edges is one **period** or **cycle**
- Used to control when values change

Clocked S-R Latch

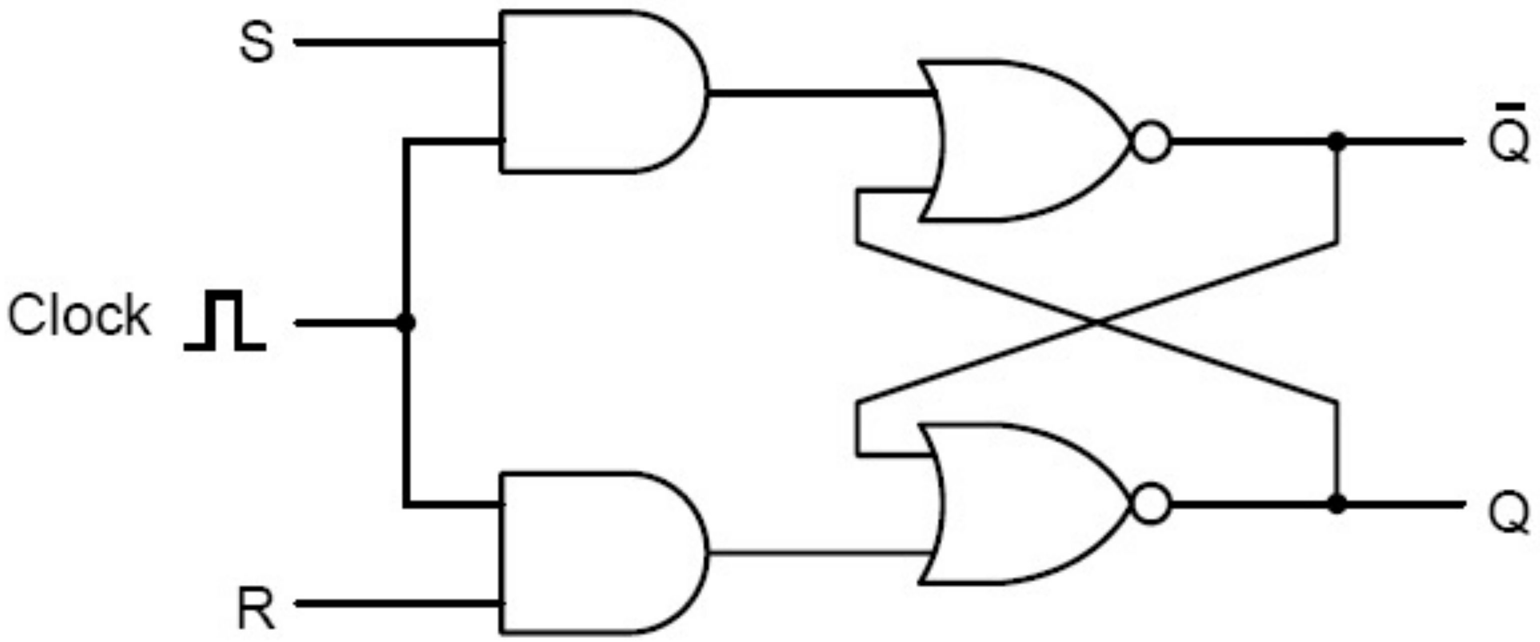


Figure 3-23. A clocked SR latch.

- Only changes state when the clock is asserted

Given S, R and Clock, Q will be:

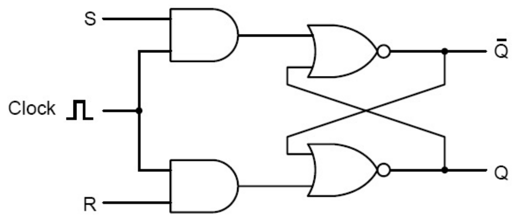
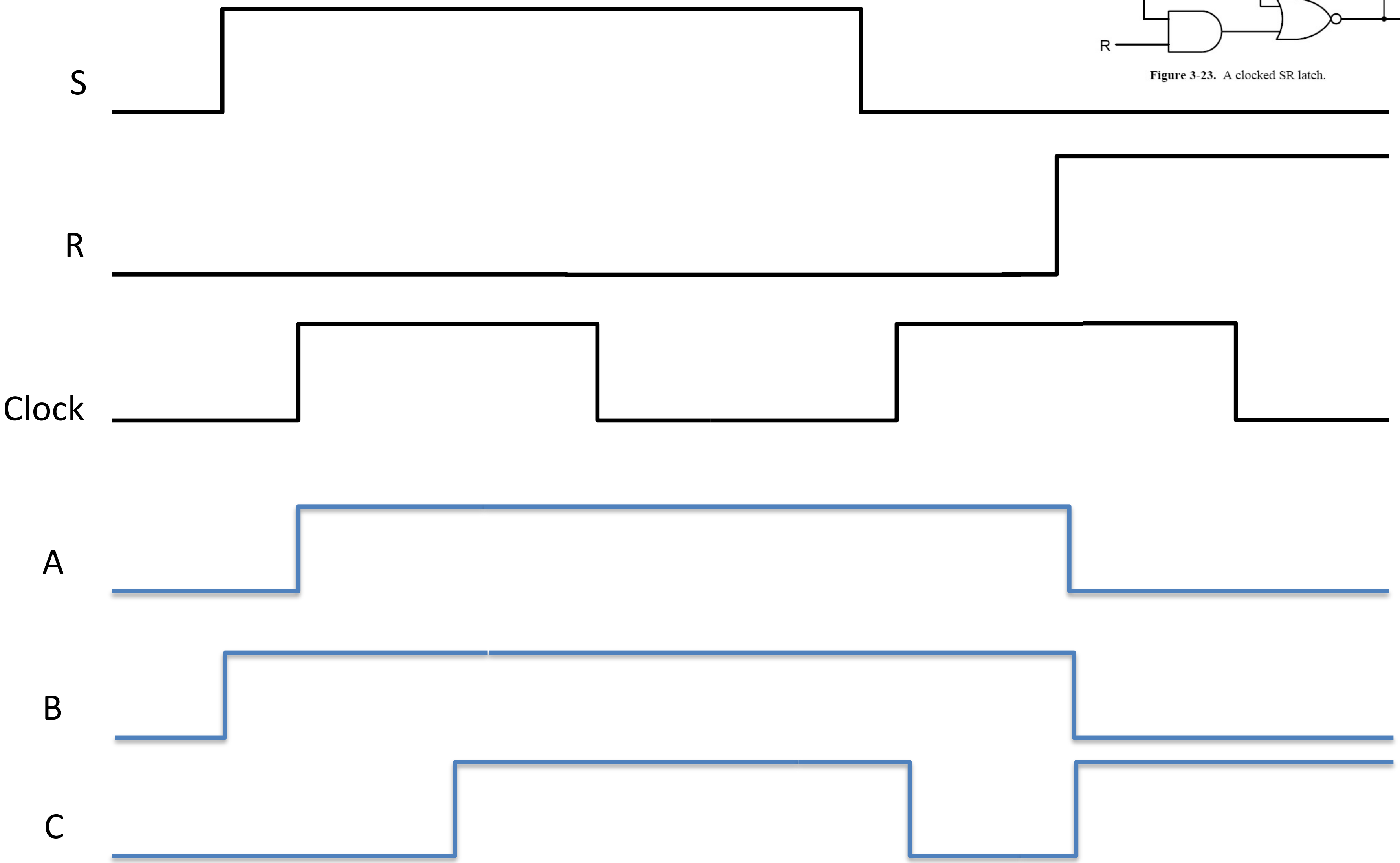
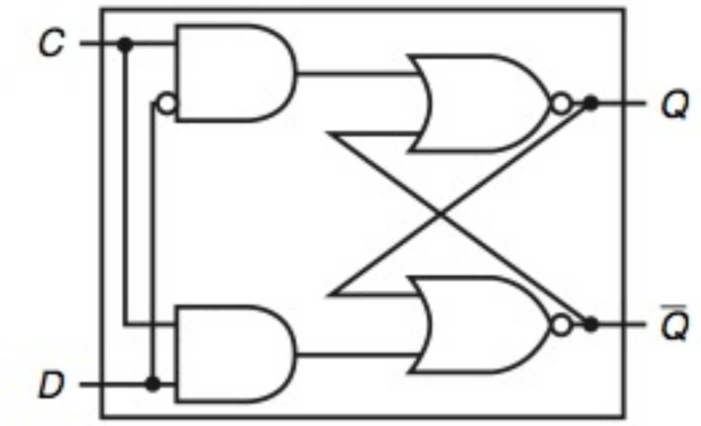


Figure 3-23. A clocked SR latch.



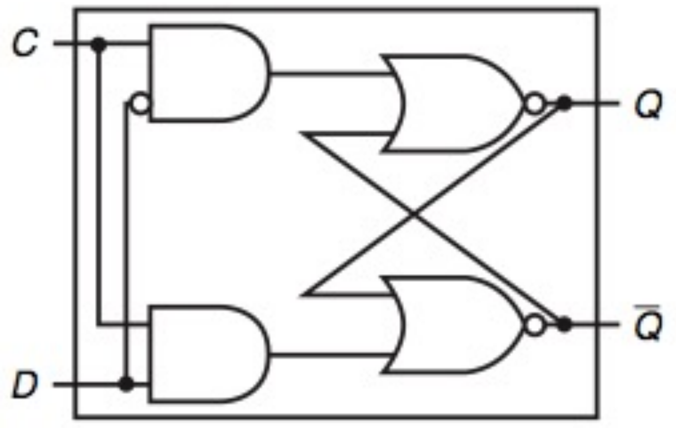
D. None of the above

Clocked D-Latch



- S-R latch, but now there is a single input, D, ANDed with the clock (labeled C rather than the more normal clk)
- Now impossible to have both inputs set to 1

Which Column Completes the Truth Table?

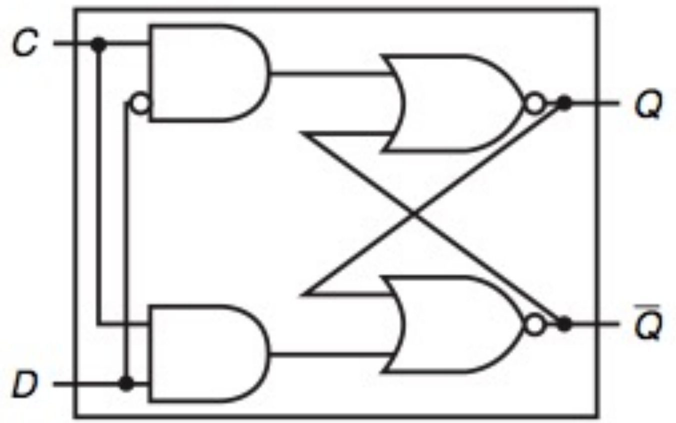


C	D	Q
1	1	
1	0	

A	B	C	D
1	1	0	1
1	0	1	Q_{prev}

E. None of the above

Which Column Completes the Truth Table?

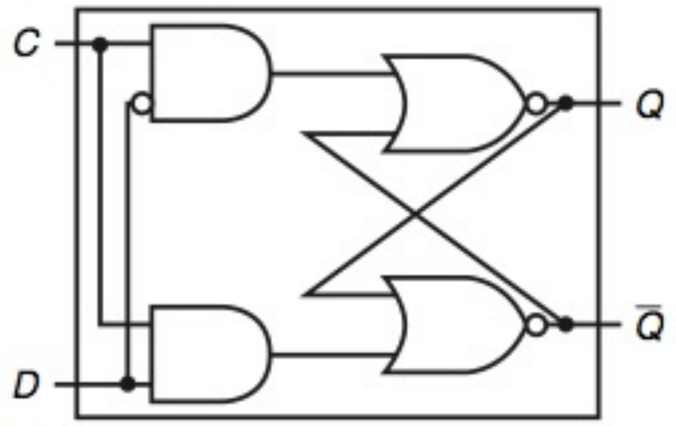


C	D	Q
0	1	
0	0	

A	B	C	D
0	1	1	Q_{prev}
0	0	Q_{prev}	Q_{prev}

E. None of the above

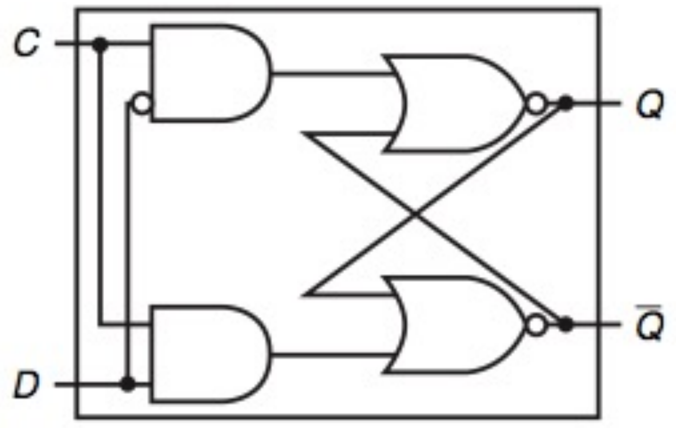
Clocked D-Latch

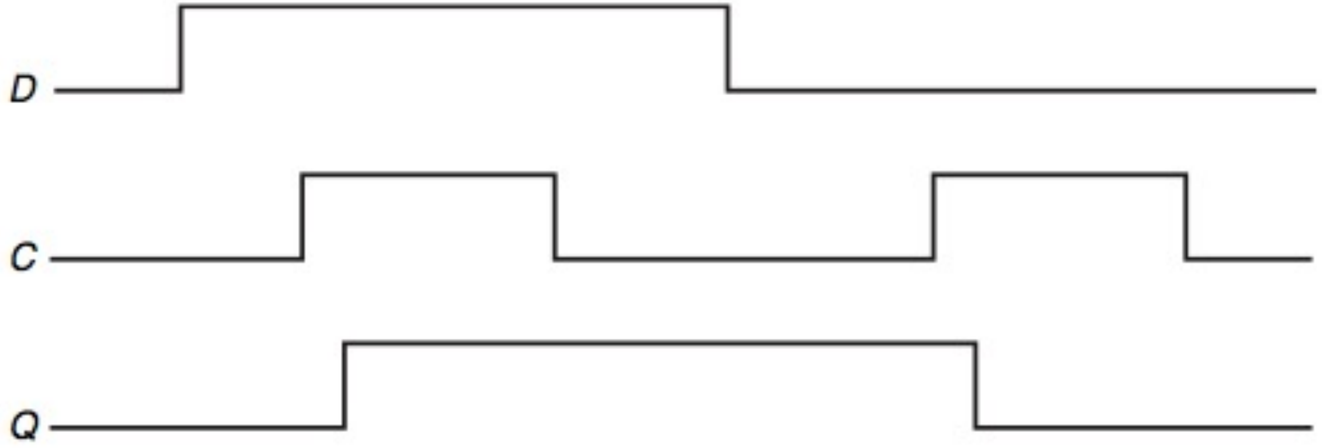


- Latch is “open” when clock is asserted (asserted = logical 1)

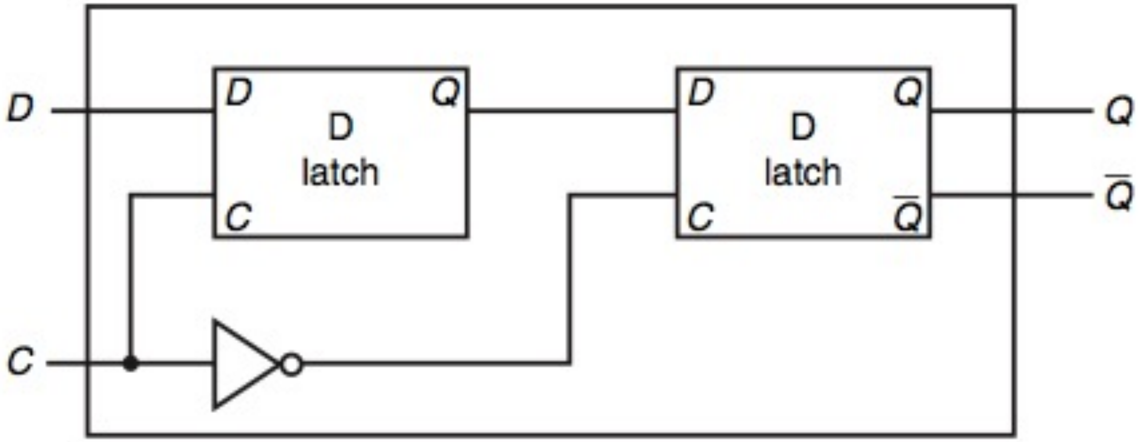
- Q = value of D when the latch is open
  Q = most recently set value when the latch is closed

Clocked D-Latch; note output takes a little time to change after the clock goes high



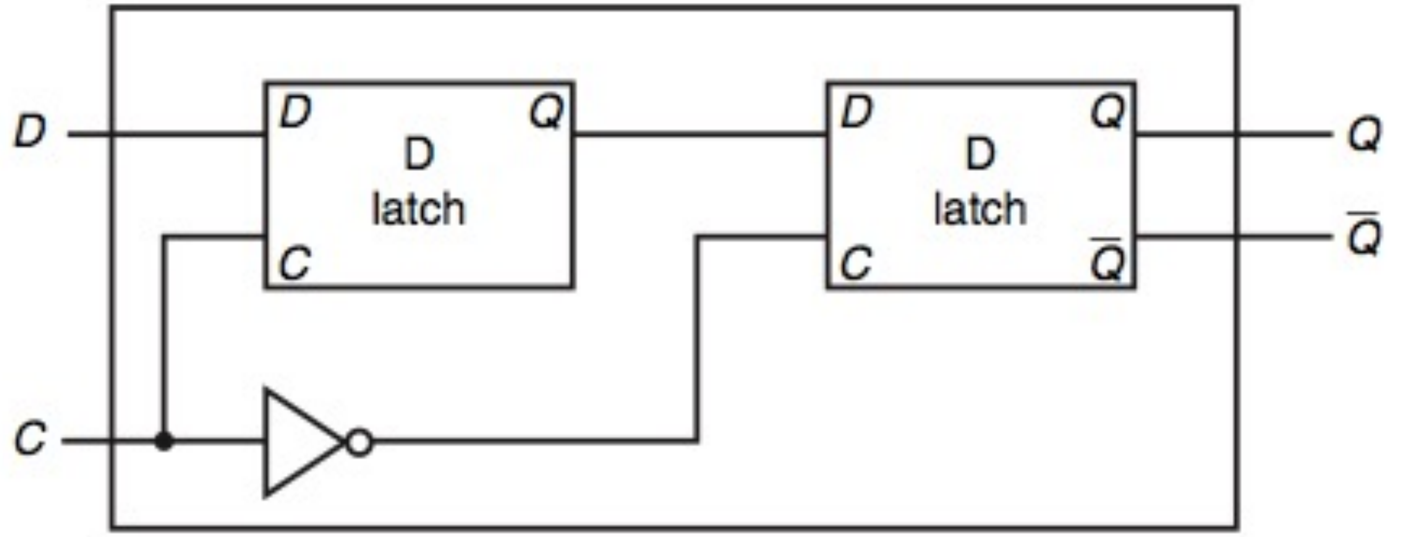


D Flip-Flop



- Two D-Latches, with the clock negated to the second latch

The value of (the right-most) Q can change



A. Any time the clock is 1.

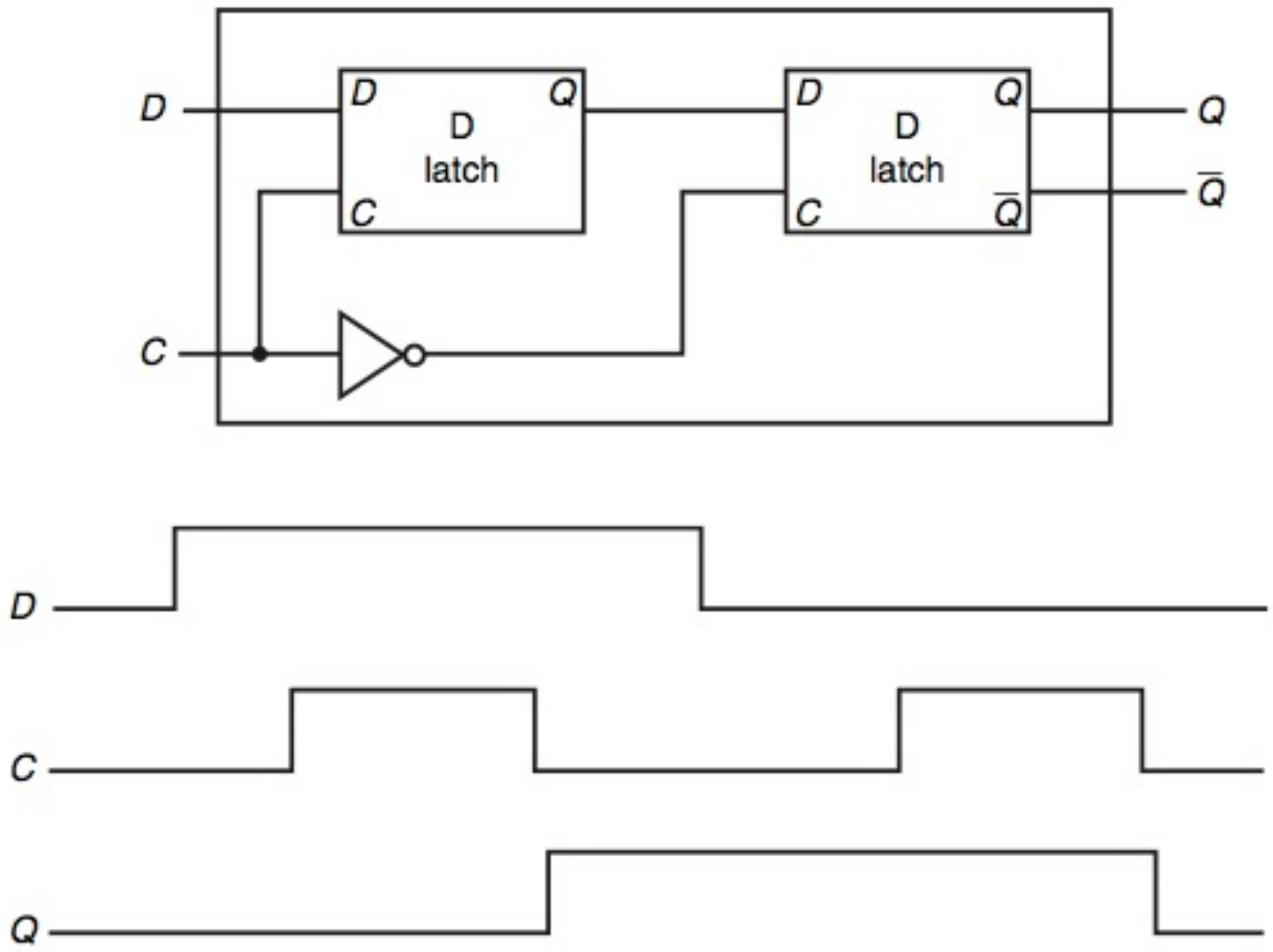
B. Any time the clock is 0.

C. When the clock changes from 1 to 0.

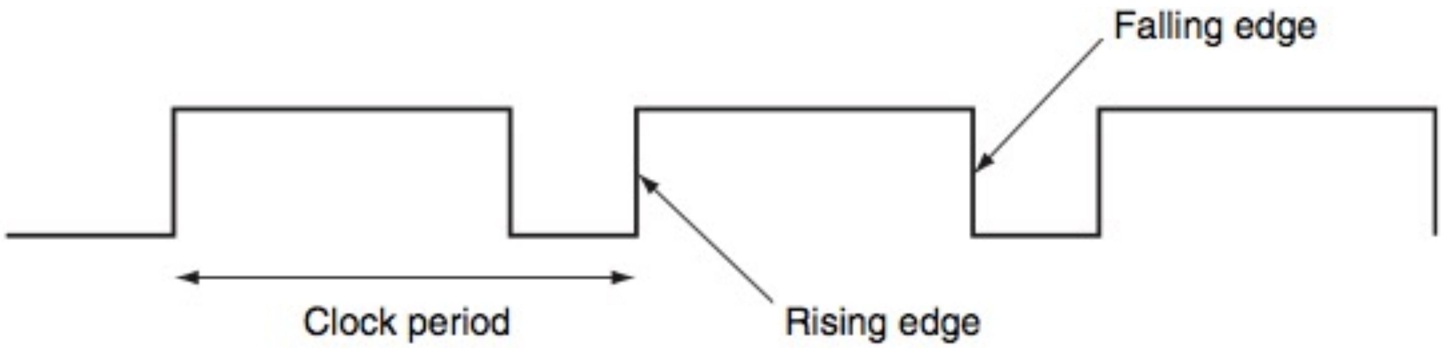
D. When the clock changes from 0 to 1.

E. None of the above

D-flip-flop: Falling Edge Trigger



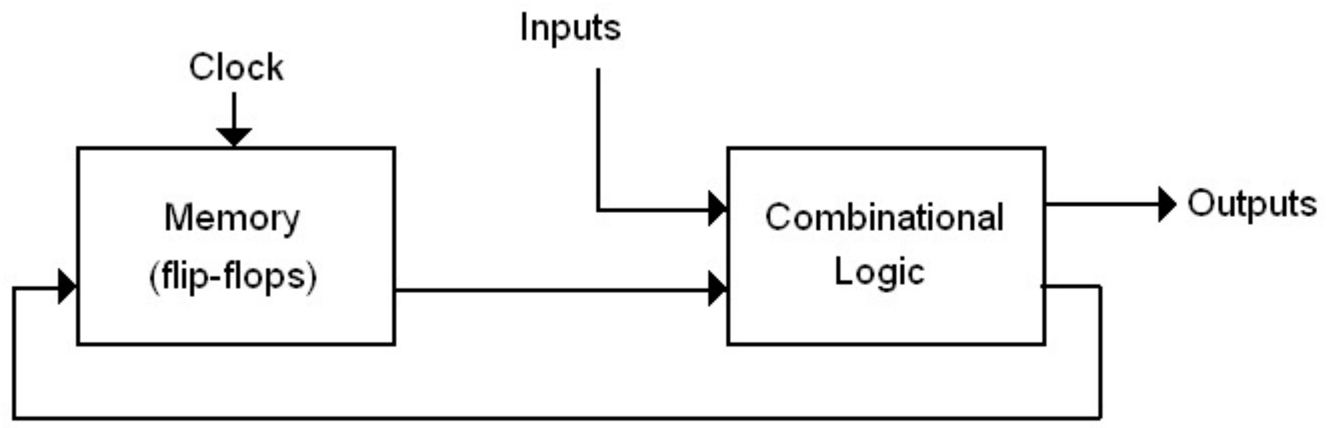
Edge-triggering



- All changes to state happen at one point in the clock cycle (either rising edge, or falling edge).

- (This is an unusual clock with a 75% duty cycle—it's on 75% of the time—most clocks have a 50% duty cycle)

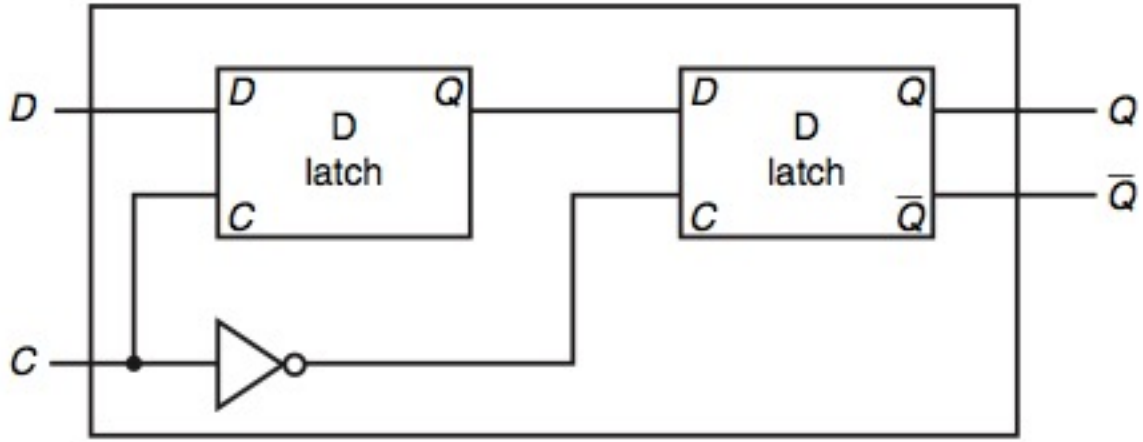
Memory



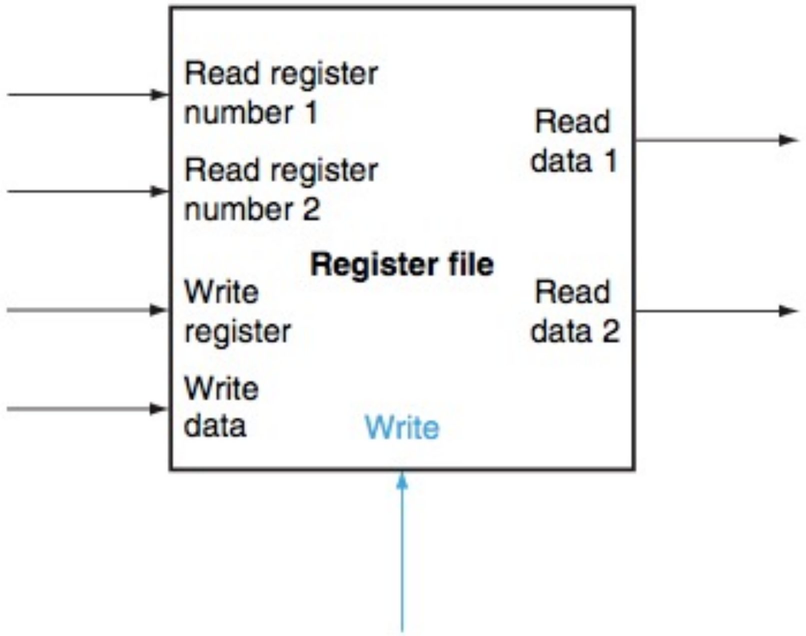
- Can save the results of combinational logic (think the ALU)
- Registers are (multi-bit) flip-flops!

Registers

- Each 32-bit register will consist of 32 1-bit D flip-flops

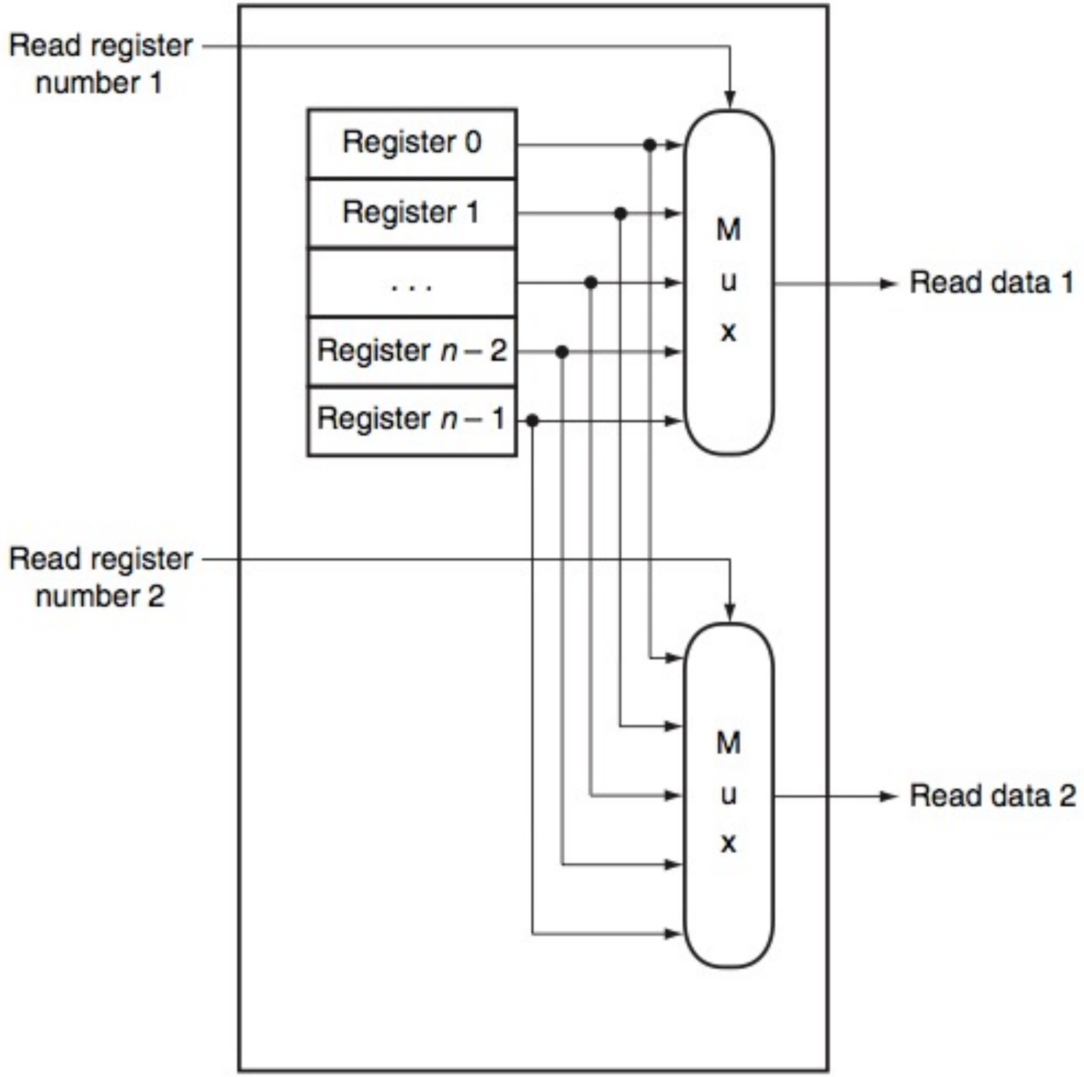


Register File

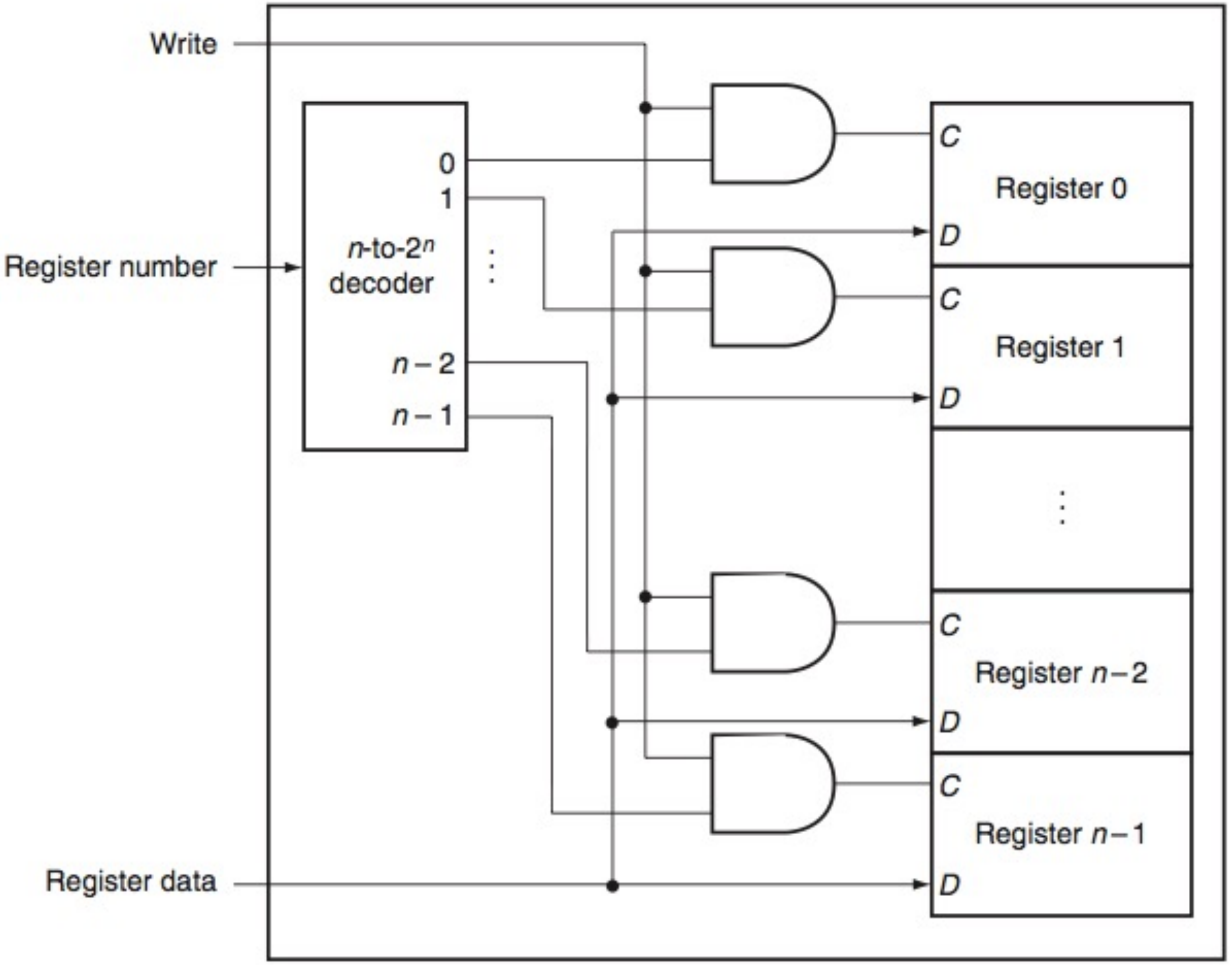


- Set of registers that can be written/read by supplying a register number
- MIPS has a register file with thirty-two 32-bit registers

Read Function



Write Function



*The image is not quite correct. It should be a lg n to n decoder

In MIPS, we have 32 registers so we need a 5-to-32 decoder, not a 32-to-4294967296 decoder!

What will happen if we read and write to a register in the same clock cycle?

A. The read will get the original value

B. The read will get the just written value

C. It is ambiguous

D. None of the above

Reading

- Next lecture: Floating Point
  - 4.4

- Problem Set 6 due Friday